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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,364	07/23/2001	Tony G. Ivanov	42024/MJM/A717	3384

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EXAMINER

FOONG, SUK SAN

ART UNIT	PAPER NUMBER
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2823

DATE MAILED: 06/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/911,364

Applicant(s)

IVANOV ET AL.

Examiner

Suk-San Foong

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 4/2/03.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 and 32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 and 32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 6 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The step recited in claim 6 is recited in claim 1, lines 7-9.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4, 7-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 4, line 2, it is questioned whether “conductive materials” are the same conductive materials recited in claim 1, line 8. For the purposes of the rejections below, the recited “conductive materials in claim 4, line 2 has been treated as if they are the same conductive materials recited in claim 1, line 8.

5. Claim 5, line 6, claim 7, line 6, it appears that “said conductive material,” should be deleted.

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6. Claim 9, lines 1-2, it appears that either “said horizontal sections of conductive material, and said vertical sections of said conductive materials” or “said conductive cover layer and said side conductive materials” should be deleted since “said horizontal sections of conductive material” and “said vertical sections of said conductive materials” corresponds to “said conductive cover layer” and “said side conductive materials”, respectively.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1-8, 10-14, 21, 22 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. ('495), Fujii ('223) and Czagas et al. ('200).

Saito et al. discloses a method of forming integrated circuit devices with plurality of isolated silicon regions which includes providing substructure having silicon substrate 10 and trenches 11 thereby forming a group of first plurality of isolated silicon sections (Col. 5, lines 3-12, and Fig. 3), subsequently forming insulating layer 3 over the group of first plurality of isolated silicon sections (Col. 5, lines 13-15, and Fig. 4), subsequently depositing material 12 such as polysilicon over substrate 10 including trenches 11 such that material 12 extends in both horizontal and vertical directions thereby enclosing the group of first plurality of isolated silicon sections (Col. 5, lines 35-37), then bonding the substructure with material 12 to semiconductor substrate 1 (Col. 5, lines 46-49, and Fig. 7), subsequently separating a portion of the substructure through grinding followed by polishing (Col. 5, lines 51-67), and then forming transistor elements in the group of first plurality of isolated silicon sections 4 (Col. 6, lines 38-40).

Saito et al. does not disclose that a conductive material bounds the horizontal and vertical sections of the isolated silicon sections.

Saito et al. does not disclose that providing a semiconductor substrate having an insulating layer.

Saito et al. does not disclose forming interconnect leads extending through openings of side conductive materials as recited in claim 21, lines 2-3.

Fujii discloses a method of forming a semiconductor device with conductive polysilicon layers covering horizontal and vertical portion of each SOI region (Col. 7, lines 23-27) which includes providing a substructure comprising semiconductor substrate 1 having silicon dioxide layer 3, silicon nitride layer 4 and conductive cover layer 5 such as doped polysilicon (Col. 7, line 63 to Col. 8, line 9, and Fig. 2A), providing semiconductor substrate 6 having insulating

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layer 7 such as silicon dioxide and a top surface (Col. 8, lines 21-26, and Fig. 2B), subsequently bonding the top surface of semiconductor substrate 6 with the substructure (Col. 8, lines 29-36, and Fig. 3), then etching through the substructure to form trench 8 thereby forming a group of first plurality of isolated silicon sections (Col. 8, lines 50-57, and Fig. 4), subsequently forming insulating materials 9 over the group of first plurality of isolated silicon sections (Col. 8, lines 60-63, and Fig. 5), subsequently filling trenches with conductive materials 5, thus, forming side conductive materials 5 (Col. 7, lines 23-27, Col. 9, lines 10-13, and Fig. 7), and then forming semiconductor elements in and on the group of first plurality of isolated silicon sections such as forming interconnect leads 13 through side conductive materials (Col. 9, lines 23-28, and Fig. 1).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Saito et al. with Fujii because it would enable formation of material 12 of Saito et al. to be performed and obtain further advantage of electrically stabilizing the plurality of isolated silicon sections (Fujii, Col. 7, lines 28-32).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Saito et al. with Fujii because it would enable the step of bonding the substructure with material 12 to semiconductor substrate 1 of Saito et al. to be performed.

It would have been within the scope to one ordinary skill in the art to combine the teachings of Saito et al. with Fujii because it would enable formation the integrated circuit devices of Saito et al. to be performed.

In regard to claim 5, the step recited in line 7 would be obtained as the same materials are being treated the same as the instant invention.

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The combination process does not disclose the substructure having a bottom portion formed of a dielectric film.

Czagas et al. teaches forming an insulating layer 18.2 over a doped polysilicon layer 18.1 prior to bonding with a handle wafer (Paragraph [0036], and Figs. 6A to 6D).

It would have been within the scope to one ordinary skill in the art to combine the teachings of the combination process with Czagas et al. because it would enable forming insulating layer such as silicon dioxide over material 12 of the combination process to be performed.

10. Claims 15-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. ('495), Fujii ('223) and Czagas et al. ('200) as applied to claims 1-8, 10-14, 21, 22 and 32 above, and further in view of Bruel et al.

Bruel et al. discloses a method of forming SOI substrate which includes providing a substructure A with insulating layer, then implanting hydrogen into an upper region of substructure A, then hydrophilic bonding substructure A with semiconductor substrate B, subsequently separating a portion of the substructure A at a temperature within the range of 400°C to 600°C, and then polishing the surface of substructure A (p. 178).

It would have been within the scope to one ordinary skill in the art to combine the teachings of the combination process because it would enable the step of separating a portion of the substructure of the combination process to be performed.

11. Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. ('495), Fujii ('223) and Czagas et al. ('200) as applied to claims 1-8, 10-14, 21, 22 and 32 above, and further in view of Gauthier, Jr. et al. ('742).

The combination process does not disclose that the conductive material is comprised of tungsten.

Gauthier, Jr. et al. discloses forming isolation structures in semiconductor devices by filling the isolation structures after trench etching with conductive material such as doped polysilicon and tungsten (Col. 2, lines 45-55, Col. 4, lines 30-44, and Figs. 1A and 1B).

It would have been within the scope to one ordinary skill in the art to combine the teachings of the combination process with Gauthier, Jr. et al. because it would enable formation of material 12 in trenches 11 of the combination process to be performed.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after

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the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suk-San Foong whose telephone number is 703-305-0383. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 (7724, 3431, 3432).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

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June 16, 2003


George Fourson
Primary Examiner
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